



Docket No. 1303.026US1
WD # 448058

Micron Ref. No. 01-0516

Clean Version of Pending Claims

HIGHLY RELIABLE AMORPHOUS HIGH-K GATE OXIDE ZrO₂

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Serial No.: 09/945,535

Claims 1-2, 4-10, 12-15, 17-23, 25-31, 33-37, 51-52, and 54-56, as of December 31, 2002
(date of response to second office action filed).

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1. (Amended) A method of forming a gate oxide on a transistor body region, comprising:
evaporation depositing a metal layer on the body region using electron beam evaporation,
the metal being chosen from the group IVB elements of the periodic table; and
oxidizing the metal layer to form a metal oxide layer on the body region.
 2. The method of claim 1, wherein evaporation depositing the metal layer includes
evaporation depositing a zirconium layer.
 4. The method of claim 3, wherein electron beam evaporation depositing the metal layer
includes electron beam evaporation of a 99.9999% pure metal target material.
 5. The method of claim 1, wherein evaporation depositing the metal layer includes
evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.
 6. The method of claim 1, wherein oxidizing the metal layer includes oxidizing at a
temperature of approximately 400 °C.
 7. The method of claim 1, wherein oxidizing the metal layer includes oxidizing with atomic
oxygen.
 8. The method of claim 1, wherein oxidizing the metal layer includes oxidizing using a
krypton (Kr)/oxygen (O₂) mixed plasma process.
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9. (Amended) A method of forming a gate oxide on a transistor body region, comprising:
evaporation depositing a metal layer on the body region using electron beam evaporation,
the metal being chosen from the group IVB elements of the periodic table; and
oxidizing the metal layer using a krypton(Kr)/oxygen (O₂) mixed plasma process to form
a metal oxide layer on the body region.

10. The method of claim 9, wherein evaporation depositing the metal layer includes
evaporation depositing a zirconium layer.

12. The method of claim 11, wherein electron beam evaporation depositing the metal layer
includes electron beam evaporation of a 99.9999% pure metal target material.

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13. The method of claim 9, wherein evaporation depositing the metal layer includes
evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

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14. (Amended) A method of forming a transistor, comprising:
forming first and second source/drain regions;
forming a body region between the first and second source/drain regions;
evaporation depositing a metal layer on the body region using electron beam evaporation,
the metal being chosen from the group IVB elements of the periodic table;
oxidizing the metal layer to form a metal oxide layer on the body region; and
coupling a gate to the metal oxide layer.

15. The method of claim 14, wherein evaporation depositing the metal layer includes
evaporation depositing a zirconium layer.

SUB 7
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17. The method of claim 16, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

18. The method of claim 14, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

19. The method of claim 14, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

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20. The method of claim 14, wherein oxidizing the metal layer includes oxidizing with atomic oxygen. D

21. The method of claim 14, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O₂) mixed plasma process.

22. (Amended) A method of forming a memory array, comprising:

forming a number of access transistors, comprising:

forming first and second source/drain regions;

forming a body region between the first and second source/drain regions;

evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;

oxidizing the metal layer to form a metal oxide layer on the body region;

coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors; and

PENDING CLAIMS

Page 4

Docket No. 1303.026US1

Micron Ref. No. 01-0516

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SUB 7
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forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors.

23. The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

25. The method of claim 24, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

26. The method of claim 22, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

27. The method of claim 22, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

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28. The method of claim 22, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

29. The method of claim 22, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O₂) mixed plasma process.

30. (Amended) A method of forming an information handling system, comprising:
forming a processor;
forming a memory array, comprising:
forming a number of access transistors, comprising:
forming first and second source/drain regions;
forming a body region between the first and second source/drain regions;

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evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;
oxidizing the metal layer to form a metal oxide layer on the body region;
coupling a gate to the metal oxide layer;

forming a number of wordlines coupled to a number of the gates of the number of access transistors;

forming a number of sourcelines coupled to a number of the first source/drain regions of the number of access transistors;

forming a number of bitlines coupled to a number of the second source/drain regions of the number of access transistors; and

forming a system bus that couples the processor to the memory array.

31. The method of claim 30, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

33. The method of claim 32, wherein electron beam evaporation depositing the metal layer includes electron beam evaporation of a 99.9999% pure metal target material.

34. The method of claim 30, wherein evaporation depositing the metal layer includes evaporation depositing at an approximate substrate temperature range of 150 - 400 °C.

35. The method of claim 30, wherein oxidizing the metal layer includes oxidizing at a temperature of approximately 400 °C.

36. The method of claim 30, wherein oxidizing the metal layer includes oxidizing with atomic oxygen.

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C6 51. (Amended) A transistor formed by the process, comprising:
forming a body region coupled between a first source/drain region and a second source/drain region;
evaporation depositing a metal layer on the body region using electron beam evaporation, the metal being chosen from the group IVB elements of the periodic table;
oxidizing the metal layer to form a metal oxide layer on the body region; and
coupling a gate to the metal oxide layer.

D 52. The transistor of claim 51, wherein evaporation depositing the metal layer includes evaporation depositing a zirconium layer.

54. The method of claim 51, wherein oxidizing the metal layer includes oxidizing using a krypton (Kr)/oxygen (O₂) mixed plasma process.

C7 55. (Amended) A method of forming a gate oxide on a transistor body region, comprising:
electron beam evaporation depositing a zirconium layer on the body region; and
oxidizing the zirconium layer to form a metal oxide layer on the body region.

56. (Amended) The method of claim 55, wherein oxidizing the zirconium layer includes oxidizing a zirconium layer to form an oxide with a conduction band offset in a range of approximately 5.16 eV to 7.8 eV.